Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (original) An integrated circuit comprising:

at least one intra-chip driver or receiver connected through a post-passivation interconnection system to elsewhere on said integrated circuit.

2. (currently amended) The ~~intergrated~~ integrated circuit according to Claim 1 further comprising:

a fine line metallization system formed over a semiconductor substrate in one or more thin layers of dielectric;

a passivation layer over said fine line metallization system;

a thick, wide metallization system formed above said passivation layer, in one or more thick layers of dielectric; and

said post-passivation interconnect system wherein said thick layers of dielectric are thicker than said thin layers of dielectric, wherein said thick, wide metallization system is used as a distribution network for an electrical stimulus, and wherein said thick, wide metallization system is connected to said at least one intra-chip driver or receiver.

3. (original) The integrated circuit according to Claim 2 further comprising one or more internal circuits comprising one or more active devices formed in and on said semiconductor substrate wherein said thick, wide metallization system is connected to said internal circuits.

4. (original) The integrated circuit according to Claim 2 further comprising one or more off-chip drivers and/or receivers and/or I/O circuits formed in and on said semiconductor substrate wherein said thick, wide metallization system is connected to said one or more off-chip drivers and/or receivers and/or I/O circuits.

5. (original) The integrated circuit according to Claim 2 further comprising one or more ESD circuits formed in and on said semiconductor substrate wherein said thick, wide metallization system is connected to said one or more ESD circuits.

6. (original) The integrated circuit according to Claim 2 further comprising one or more repeaters formed in and on said semiconductor substrate wherein each of said repeaters comprises a receiver and an intra-chip driver wherein said thick, wide metallization system is connected to said one or more repeaters.

7. (original) The integrated circuit according to Claim 1 further comprising power/ground connections to said at least one intra-chip driver or receiver wherein said power/ground connections are distributed through said post-passivation interconnect system.

8. (original) A chip structure, comprising:

one or more internal circuits comprising one or more active devices formed in and on a semiconductor substrate;

one or more ESD circuits formed in and on said semiconductor substrate;

one or more intra-chip drivers and/or receivers formed in and on said semiconductor substrate;

one or more off-chip drivers and/or receivers and/or I/O circuits formed in and on said semiconductor substrate;

a fine line metallization system, formed over said semiconductor substrate in one or more thin layers of dielectric;

a passivation layer over said fine line metallization system;

a thick, wide metallization system formed above said passivation layer, in one or more thick layers of dielectric; and

a post-passivation interconnect scheme wherein said thick layers of dielectric are thicker than said thin layers of dielectric, wherein said thick, wide metallization system is used as a distribution network for an electrical stimulus, and wherein said thick, wide metallization system is connected to said one or more ESD circuits, said one or more internal circuits, said one or more intra-chip drivers and/or receivers, said one or more off-chip drivers and/or receivers and/or I/O circuits, and to at least one off-chip contact pad.

9. (original) The structure of Claim 8 wherein said distribution network is connected to said ESD circuits, to said one or more internal circuits, and to said one or more intra-chip drivers and/or receivers by vias, which are formed through said one or more thick layers of

dielectric, through said passivation layer, and through said one or more thin layers of dielectric.

10. (original) The structure of Claim 8 wherein said electrical stimulus comprises a power or ground voltage.

11. (original) The structure of Claim 8 wherein said ESD circuit is connected in parallel with said one or more internal circuits, through said distribution network.

12. (original) The structure of Claim 10 wherein said distribution network acts as a global distribution for said power or ground voltages, and said vias are further connected to local power/ground distribution networks formed in said fine line metallization system.

13. (original) The structure of Claim 8 wherein said passivation layer comprises silicon nitride having a thickness of greater than 0.4 μm.

14. (original) The structure of Claim 8 wherein said thick wide metallization system is formed in a thick polymer layer overlying said passivation layer.

15. (original) The structure of Claim 8 wherein said thick wide metallization system comprises electroplated gold or copper.

16. (original) The structure of Claim 8 wherein said electrical stimulus comprises a clock or signal voltage.

17. (original) The structure of Claim 8, further comprising off-chip driver, receiver or I/O circuits connected in series between said one or more off-chip contact pads and said distribution network.

18. (original) The structure of Claim 8 wherein said distribution network is connected to said intra-chip drivers and/or receivers and wherein said intra-chip drivers and/or receivers are further connected in series to said internal circuits.

19. (original) The structure of Claim 17 wherein said ESD circuit is connected in parallel with said off-chip driver, receiver or I/O circuits.

20. (original) The structure of Claim 17 wherein said intra-chip drivers are smaller than said off-chip drivers.

21. (original) The structure of Claim 8 wherein said intra-chip drivers and/or receivers are not connected to ESD circuits or I/O circuits.

22. (original) The structure of Claim 16 wherein said distribution network acts as a global distribution for said clock or signal voltages, and said vias through said passivation layer are

further connected to local clock/signal distribution networks formed in said fine line metallization system.

23. (original) The structure of Claim 8 wherein metal in said thick, wide metallization system is greater than about 1 micrometer in thickness.

24. (original) The structure of Claim 8 wherein said one or more thick layers of dielectric are each greater than about 2 micrometers in thickness.

25. (original) A chip structure, comprising:

one or more internal circuits comprising one or more active devices formed in and on a semiconductor substrate;

one or more ESD circuits formed in and on said semiconductor substrate;

one or more intra-chip drivers and/or receivers formed in and on said semiconductor substrate;

one or more off-chip drivers and/or receivers and/or I/O circuits formed in and on said semiconductor substrate;

a fine line metallization system, formed over said semiconductor substrate in one or more thin layers of dielectric;

a passivation layer over said fine line metallization system;

a thick, wide metallization system formed above said passivation layer, in one or more thick layers of dielectric; and

a post-passivation interconnect scheme wherein said thick layers of dielectric are thicker than said thin layers of dielectric, wherein said thick, wide metallization system is used as a distribution network for an electrical stimulus, and wherein said thick, wide metallization system is connected to said one or more ESD circuits, said one or more intra-chip drivers and/or receivers, said one or more off-chip drivers and/or receivers and/or I/O circuits, and to at least one off-chip contact pad and wherein said one or more internal circuits are connected through said fine line metallization system.

26. (original) The structure of Claim 25 wherein said distribution network is connected to said ESD circuits and to said one or more intra-chip drivers and/or receivers by vias, which are formed through said one or more thick layers of dielectric, through said passivation layer, and through said one or more thin layers of dielectric.

27. (original) The structure of Claim 25 wherein said electrical stimulus comprises a clock or signal voltage.

28. (original) The structure of Claim 25 further comprising off-chip driver, receiver or I/O circuits connected in series between said one or more off-chip contact pads and said distribution network.

29. (original) The structure of Claim 25 wherein said distribution network is connected to said intra-chip drivers and/or receivers and wherein said intra-chip drivers and/or receivers are further connected in series to said internal circuits.

30. (original) The structure of Claim 28 wherein said intra-chip drivers are smaller than said off-chip drivers.

31. (original) The structure of Claim 26 wherein said distribution network acts as a global distribution for said clock or signal voltages, and said vias through said passivation layer are further connected to local clock/signal distribution networks formed in said fine line metallization system.

32. (original) A chip structure, comprising:

one or more internal circuits comprising one or more active devices formed in and on a semiconductor substrate;

one or more intra-chip drivers and/or receivers formed in and on a semiconductor substrate;

a fine line metallization system, formed over said semiconductor substrate in one or more thin layers of dielectric;

a passivation layer over said fine line metallization system; and

a thick, wide metallization system formed above said passivation layer, in one or more thick layers of dielectric,

wherein said thick layers of dielectric are thicker than said thin layers of dielectric, wherein said thick, wide metallization system is used as a distribution network for a clock or signal voltage, and wherein said thick, wide metallization system is connected to said one or more internal circuits and to said one or more intra-chip drivers and/or receivers.

33. (original) The structure of Claim 32 wherein said distribution network is connected to said one or more internal circuits and to said one or more intra-chip drivers and/or receivers by vias, which are formed through said one or more thick layers of dielectric, through said passivation layer, and through said one or more thin layers of dielectric.

34. (original) The structure of Claim 33 wherein said distribution network acts as a global distribution for said clock or signal voltages, and said vias are further connected to local clock or signal distribution networks, respectively, formed in said fine line metallization system.

35. (original) The structure of Claim 32 wherein metal in said thick, wide metallization system is greater than about 1 micrometer in thickness.

36. (original) The structure of Claim 32 wherein said one or more thick layers of dielectric are each greater than about 2 micrometers in thickness.

37. (original) The structure of Claim 32 wherein said passivation layer comprises silicon nitride having a thickness of greater than 0.4 μm.

38. (original) The structure of Claim 32 wherein said thick wide metallization system is formed in a thick polymer layer overlying said passivation layer.

39. (original) The structure of Claim 32 wherein said thick wide metallization system comprises electroplated gold or copper.

40. (original) A chip structure, comprising:

one or more internal circuits comprising one or more active devices formed in and on a semiconductor substrate;

one or more intra-chip drivers and/or receivers formed in and on a semiconductor substrate;

a fine line metallization system, formed over said semiconductor substrate in one or more thin layers of dielectric;

a passivation layer over said fine line metallization system; and

a thick, wide metallization system formed above said passivation layer, in one or more thick layers of dielectric,

wherein said thick layers of dielectric are thicker than said thin layers of dielectric, wherein said thick, wide metallization system is used as a distribution network for a clock or signal voltage, and wherein said thick, wide metallization system is connected to said one or more intra-chip drivers and/or receivers and wherein said one or more internal circuits are connected through said fine line metallization system.

41. (original) A chip structure, comprising:

one or more internal circuits comprising one or more active devices formed in and on a semiconductor substrate;

a passivation layer over one or more internal circuits; and

a thick, wide metallization system formed above said passivation layer, in one or more thick layers of dielectric,

wherein said thick, wide metallization system is used as a distribution network for an electrical stimulus.

42. (original) The structure of Claim 41 wherein said thick, wide metallization system is connected to said one or more internal circuits.

43. (original) The structure of Claim 41 wherein said passivation layer comprises silicon nitride having a thickness of greater than 0.4 μm.

44. (original) The structure of Claim 41 wherein said thick wide metallization system is formed in a thick polymer layer overlying said passivation layer.

45. (original) The structure of Claim 41 wherein said thick wide metallization system comprises electroplated gold or copper.

46. (original) The structure of Claim 41 wherein said electrical stimulus comprises a power or ground voltage.

47. (original) The structure of Claim 41 wherein said thick, wide metallization system is connected to said one or more internal circuits by vias, which are formed through said one or more thick layers of dielectric, through said passivation layer, and through said one or more thin layers of dielectric.

48. (original) The structure of Claim 41 further comprising one or more intra-chip drivers and/or receivers wherein said one or more internal circuits and said one or more intra-chip drivers and/or receivers are connected.

49. (original) The structure of Claim 48 wherein said one or more internal circuits and said one or more intra-chip drivers and/or receivers are connected in parallel by vias through said wide, thick metallization system.

50. (original) The structure of Claim 47 wherein said one or more internal circuits and said one or more intra-chip drivers and/or receivers are connected by vias, which are formed through said one or more thick layers of dielectric, and through said passivation layer.

51. (original) The structure of Claim 41 further comprising off-chip driver, receiver or I/O circuits connected in series between one or more off-chip contact pads and said distribution network.

52. (original) The structure of Claim 48 further comprising an ESD circuit connected in parallel with said off-chip driver, receiver or I/O circuits.

53. (original) The structure of Claim 48 wherein said intra-chip drivers are smaller than said off-chip drivers.

54. (original) The structure of Claim 48 wherein said intra-chip drivers and/or receivers are not connected to ESD circuits or I/O circuits.

55. (original) The structure of Claim 41 further comprising a fine line metallization system formed in said one or more thin layers of dielectric underlying said passivation layer wherein said distribution network acts as a global distribution for said clock or signal voltages, and said distribution network is further connected to local clock/signal distribution networks formed in said fine line metallization system through vias in said thick , wide metallization system and in said passivation layer.

56. (original) The structure of Claim 55 further comprising one or more intra-chip drivers and/or receivers wherein said one or more internal circuits and said one or more intra-chip drivers and/or receivers are connected in series by said fine line metallization system.

57. (original) The structure of Claim 41 wherein metal in said thick, wide metallization system is greater than about 1 micrometer in thickness.

58. (original) The structure of Claim 41 wherein said one or more thick layers of dielectric are each greater than about 2 micrometers in thickness.

59. (original) A method of forming a post passivation interconnection, comprising:

forming at least one intra-chip driver or receiver connected through a post-passivation interconnection system to elsewhere on said integrated circuit.

60. (original) The method according to Claim 59 further comprising:

forming a fine line metallization system over a semiconductor substrate in one or more thin layers of dielectric;

forming a passivation layer over said fine line metallization system; and

forming a thick, wide metallization system above said passivation layer, in one or more thick layers of dielectric

wherein said post-passivation interconnect system comprises said thick layers of dielectric thicker than said thin layers of dielectric, wherein said thick, wide metallization system is used as a distribution network for an electrical stimulus, and wherein said thick, wide metallization system is connected to said at least one intra-chip driver or receiver.

61. (original) The method according to Claim 60 further comprising forming one or more internal circuits comprising one or more active devices in and on said semiconductor substrate wherein said thick, wide metallization system is connected to said internal circuits.

62. (original) The method according to Claim 60 further comprising forming one or more off-chip drivers and/or receivers and/or I/O circuits in and on said semiconductor substrate wherein said thick, wide metallization system is connected to said one or more off-chip drivers and/or receivers and/or I/O circuits.

63. (original) The method according to Claim 60 further comprising forming one or more ESD circuits in and on said semiconductor substrate wherein said thick, wide metallization system is connected to said one or more ESD circuits.

64. (original) The method according to Claim 60 further comprising forning one or more repeaters in and on said semiconductor substrate wherein each of said repeaters comprises a receiver and an intra-chip driver wherein said thick, wide metallization system is connected to said one or more repeaters.

65. (original) The method according to Claim 60 further comprising forming power/ground connections to said at least one intra-chip driver or receiver wherein said power/ground connections are distributed through said post-passivation interconnect system.

66. (original) A method of forming a post passivation interconnection, comprising:

providing one or more internal circuits comprising one or more active devices in and on a semiconductor substrate;

providing one or more ESD circuits formed in and on said semiconductor substrate;

providing a fine line metallization system over said semiconductor substrate in one or more thin layers of dielectric;

depositing a passivation layer over said fine line metallization system; and

forming a thick, wide metallization system above said passivation layer, in one or more thick layers of dielectric,

wherein said thick layers of dielectric are thicker than said thin layers of dielectric, wherein said thick, wide metallization system is used as a distribution network for an electrical stimulus, and wherein said thick, wide metallization system is connected to said one or more ESD circuits, said one or more internal circuits, and to at least one off-chip contact pad.

67. (original) The method of Claim 66 wherein said distribution network is connected to said ESD circuits and to said one or more internal circuits by vias, which are formed through said one or more thick layers of dielectric, through said passivation layer, and through said one or more thin layers of dielectric.

68. (original) The method of Claim 66 wherein said electrical stimulus comprises a power or ground voltage.

69. (original) The method of Claim 66 wherein said ESD circuit is connected in parallel with said one or more internal circuits, through said distribution network.

70. (original) The method of Claim 66 wherein said distribution network acts as a global distribution for said power or ground voltages, and said vias are further connected to local power/ground distribution networks formed in said fine line metallization system.

71. (original) The method of Claim 66 wherein said electrical stimulus comprises a clock or signal voltage.

72. (original) The method of Claim 66 further comprising providing one or more intra-chip drivers and/or receivers wherein said one or more intra-chip drivers and/or receivers are connected by vias which are formed through said one or more thick layers of dielectric and through said passivation layer.

73. (original) The method of Claim 66 further comprising connecting off-chip driver, receiver or I/O circuits in series between said one or more off-chip contact pads and said distribution network.

74. (original) The method of Claim 70 wherein said intra-chip drivers are smaller than said off-chip drivers.

75. (original) The method of Claim 70 wherein said intra-chip drivers and/or receivers are not connected to ESD circuits or I/O circuits.

76. (original) The method of Claim 66 wherein said ESD circuit is connected in parallel with said off-chip driver, receiver or I/O circuits, through said distribution network.

77. (original) The method of Claim 66 wherein said distribution network acts as a global distribution for said clock or signal voltages, and said vias are further connected to local clock/signal distribution networks formed in said fine line metallization system.

78. (original) The method of Claim 66 wherein metal in said thick, wide metallization system comprises electroplated gold or copper formed to a thickness of greater than about 1 micrometer.

79. (original) The method of Claim 66 wherein said one or more thick layers of dielectric is each formed to a thickness of greater than about 2 micrometers.

80. (original) The method of Claim 66 wherein said one or more thick layers of dielectric comprise a polymer.

81. (original) The method of Claim 66 wherein said passivation layer comprises silicon nitride having a thickness of greater than 0.4μm.

82. (original) A method of forming a post passivation interconnection, comprising:

providing one or more internal circuits comprising one or more active devices in and on a semiconductor substrate;

providing one or more intra-chip drivers and/or receivers in and on a semiconductor substrate;

providing a fine line metallization system, over said semiconductor substrate in one or more thin layers of dielectric;

depositing a passivation layer over said fine line metallization system; and

forming a thick, wide metallization system above said passivation layer, in one or more thick layers of dielectric, wherein said thick layers of dielectric are thicker than said thin layers of dielectric, wherein said thick, wide metallization system is used as a distribution network for a clock or signal voltage, and wherein said thick, wide metallization system is connected to said one or more internal circuits and to said one or more intra-chip drivers and/or receivers.

83. (original) The method of Claim 82 wherein said distribution network is connected to said one or more internal circuits and said one or more intra-chip drivers and/or receivers by vias, which are formed through said one or more thick layers of dielectric, through said passivation layer, and through said one or more thin layers of dielectric.

84. (original) The method of Claim 82 wherein said distribution network acts as a global distribution for said clock or signal voltages, and said vias are further connected to local clock or signal distribution networks, respectively, formed in said fine line metallization system.

85. (original) The method of Claim 82 wherein metal in said thick, wide metallization system is formed to a thickness of greater than about 1 micrometer.

86. (original) The method of Claim 82 wherein said one or more thick layers of dielectric are each formed to a thickness greater than about 2 micrometers.

87. (original) The method of Claim 82 wherein said one or more thick layers of dielectric comprise a polymer.

88. (original) A method of forming a post passivation interconnection, comprising:

providing one or more internal circuits comprising one or more active devices in and on a semiconductor substrate;

depositing a passivation layer over said one or more active devices; and

forming a thick, wide metallization system above said passivation layer, in one or more thick layers of dielectric,

wherein said thick, wide metallization system is used as a distribution network for an electrical stimulus.

89. (original) The method of Claim 88 wherein said thick, wide metallization system is connected to said one or more internal circuits by vias which are formed through said one or more thick layers of dielectric and through said passivation layer.

90. (original) The method of Claim 88 wherein said electrical stimulus comprises a power or ground voltage.

91. (original) The method of Claim 88 further comprising forming one or more intra-chip drivers and/or receivers wherein said one or more intra-chip drivers and/or receivers are connected by vias which are formed through said one or more thick layers of dielectric and through said passivation layer.

92. (original) The method of Claim 88, further comprising forming off-chip driver, receiver or I/O circuits connected in series between one or more off-chip contact pads and said distribution network.

93. (original) The method of Claim 88 further comprising forming an ESD circuit connected in parallel with said off-chip driver, receiver or I/O circuits.

94. (original) The method of Claim 88 wherein said intra-chip drivers are smaller than said off-chip drivers.

95. (original) The method of Claim 93 wherein said intra-chip drivers and/or receivers are not connected to ESD circuits or I/O circuits.

96. (original) The method of Claim 88 further comprising forming a fine line metallization system in one or more thin layers of dielectric underlying said passivation layer wherein said

distribution network acts as a global distribution for said clock or signal voltages, and said vias are further connected to local clock/signal distribution networks formed in said fine line metallization system.

97. (original) The method of Claim 88 wherein metal in said thick, wide metallization system is greater than about 1 micrometer in thickness.

98. (original) The method of Claim 88 wherein said one or more thick layers of dielectric are each greater than about 2 micrometers in thickness.

99. (original) The method of Claim 88 wherein said one or more thick layers of dielectric comprise a polymer.

100. (original) A chip structure, comprising:

one or more internal circuits comprising one or more active devices formed in and on a semiconductor substrate;

one or more ESD circuits formed in and on said semiconductor substrate;

one or more intra-chip drivers and/or receivers formed in and on said semiconductor substrate;

one or more off-chip drivers and/or receivers and/or I/O circuits formed in and on said semiconductor substrate;

a fine line metallization system, formed over said semiconductor substrate in one or more thin layers of dielectric;

a passivation layer over said fine line metallization system;

a thick, wide metallization system formed above said passivation layer, in one or more thick layers of dielectric; and

a post-passivation interconnect scheme wherein said thick layers of dielectric are thicker than said thin layers of dielectric, wherein said thick, wide metallization system is used as a distribution network for an electrical stimulus, and wherein said thick, wide metallization system is connected to said one or more ESD circuits, said one or more internal circuits, said one or more intra-chip drivers and/or receivers, said one or more off-chip drivers and/or receivers and/or I/O circuits, and to at least one off-chip wire bonding contact pad and wherein connection is made between bonding wires and a metal bond pad in an opening of said passivation layer.

101. (new) A method of forming a post passivation interconnection, comprising:

providing one or more internal circuits comprising one or more active devices in and on a semiconductor substrate;

providing a fine line metallization system over said semiconductor substrate in one or more thin layers of dielectric;

depositing a passivation layer over said fine line metallization system; and

forming a thick, wide metallization system above said passivation layer in a selective deposition process, in one or more thick layers of dielectric,

wherein said thick layers of dielectric are thicker than said thin layers of dielectric, wherein said thick, wide metallization system is used as a distribution network for an electrical stimulus, and wherein said thick, wide metallization system is connected to said one or more

internal circuits, and to at least one off-chip contact pad and wherein a first product of resistance of said thick, wide metallization system times capacitance of said thick, wide metallization system is smaller than a second product of resistance of said fine line metallization system times capacitance of said fine line metallization system.

102. (new) The method of Claim 101 further comprising providing one or more intra-chip drivers and/or receivers wherein said one or more intra-chip drivers and/or receivers are connected by vias which are formed through said one or more thick layers of dielectric and through said passivation layer.

103. (new) The method of Claim 101 further comprising connecting off-chip driver, receiver or I/O circuits in series between said one or more off-chip contact pads and said distribution network.

104. (new) The method of Claim 101 further comprising providing one or more ESD circuits formed in and on said semiconductor substrate wherein said ESD circuits are connected in parallel with said off-chip driver, receiver or I/O circuits, through said distribution network.

105. (new) The method of Claim 101 wherein said passivation layer comprises silicon nitride having a thickness of greater than 0.4 μm.

106. (new) The method of claim 101 wherein silicon-based oxide is used as an intermetal dielectric material in said fine line metallization system and is deposited by chemical vapor deposition and wherein a polymer is used as an intermetal dielectric material in said post-passivation metallization system and is deposited by spin coating, by screen printing, or by laminating a dry film of said polymer to a thickness greater than about 2 micrometers.

107. (new) The method of Claim 101 wherein metal in said thick, wide metallization system is greater than about 1 micrometer in thickness.

108. (new) The method of Claim 101 wherein said one or more thick layers of dielectric are each greater than about 2 micrometers in thickness.

109. (new) The method of Claim 101 wherein said selective deposition process for forming metal lines in said thick, wide metallization comprises:

sputtering an electroplating seed layer in first openings in said passivation layer;

depositing a layer of photoresist over said electroplating seed layer;

forming second openings in said photoresist over said first openings;

electroplating a metal layer in said second openings, forming metal lines;

removing said photoresist; and

removing said electroplating seed layer in areas not covered by said metal lines.

110. (new) The method of Claim 101 wherein said fine line metallization is formed of aluminum and wherein said thick, wide metallization is formed of copper or gold.

111. (new) The method of Claim 101 wherein said fine line metallization is formed of copper and wherein said thick, wide metallization is formed of gold.

112. (new) A chip structure comprising:

one or more internal circuits comprising one or more active devices in and on a semiconductor substrate;

a fine line metallization system over said semiconductor substrate in one or more thin layers of dielectric;

a passivation layer over said fine line metallization system; and

a thick, wide metallization system above said passivation layer, in one or more thick layers of dielectric,

wherein said thick layers of dielectric are thicker than said thin layers of dielectric, wherein said thick, wide metallization system is used as a distribution network for an electrical stimulus, and wherein said thick, wide metallization system is connected to said one or more internal circuits and wherein a first product of resistance of said thick, wide metallization system times capacitance of said thick, wide metallization system is smaller than a second product of resistance of said fine line metallization system times capacitance of said fine line metallization system.

113. (new) The structure of Claim 112 further comprising one or more intra-chip drivers and/or receivers wherein said one or more intra-chip drivers and/or receivers are connected

by vias which are formed through said one or more thick layers of dielectric and through said passivation layer.

114. (new) The structure of Claim 112 further comprising off-chip driver, receiver or I/O circuits connected in series between said one or more off-chip contact pads and said distribution network.

115. (new) The structure of Claim 112 further comprising one or more ESD circuits formed in and on said semiconductor substrate wherein said ESD circuits are connected in parallel with said off-chip driver, receiver or I/O circuits, through said distribution network.

116. (new) The structure of Claim 101 wherein said passivation layer comprises silicon nitride having a thickness of greater than 0.4 μm.

117. (new) The structure of Claim 112 wherein silicon-based oxide is used as an intermetal dielectric material in said fine line metallization system and wherein a polymer is used as an intermetal dielectric material in said post-passivation metallization system and wherein said polymer has a thickness greater than about 2 micrometers.

118. (new) The structure of Claim 112 wherein metal in said thick, wide metallization system is greater than about 1 micrometer in thickness.

119. (new) The structure of Claim 112 wherein said one or more thick layers of dielectric are each greater than about 2 micrometers in thickness.

120. (new) The structure of Claim 112 wherein said fine line metallization is formed of aluminum and wherein said thick, wide metallization is formed of copper or gold.

121. (new) The structure of Claim 112 wherein said fine line metallization is formed of copper and wherein said thick, wide metallization is formed of gold.